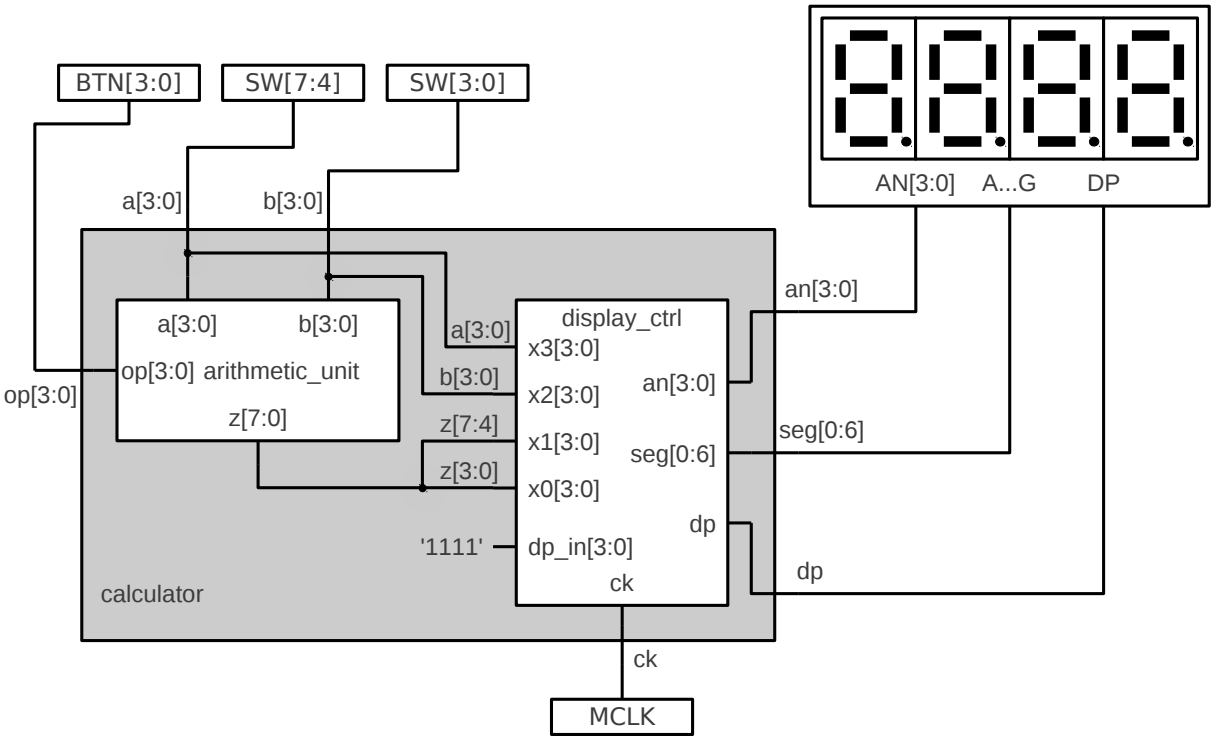
Full name: _____

Design of a simple hexadecimal calculator

Material

- Computer with Xilinx's ISE software installed.
- Digilent's Basys2 prototype board and documentation.
- Sample design files (lab kit).
- Files and documents can be downloaded from the course's web page.



Description

The objective of this lab is to design and implement a basic hexadecimal calculator on a FPGA prototype board. The calculator takes two 4-bit input numbers 'a' and 'b' and does four different operations controlled by a 4-bit signal 'op' as specified by the following table:

op	result
1xxx	a + b
01xx	a – b
001x	b – a
0001	a * b
0000	0

The result of the operation is given to a 7-segment display controller that drives a four digits 7-segment display. From left to right the digits represent: 'a' (1 digit), 'b' (1 digit) and the result (2 digits). The schematic of the calculator is depicted in the figure below, including the names of the signals and the names of the ports in the Basys2 board where the inputs and outputs should be

Full name: _____

connected.

The display control module and the calculator's top level module are already designed. The display control modules is provided in already synthesized format (.ngc) with a Verilog wrapper. The student will have to finish the arithmetic circuit design as a pre-lab work.

Pre-lab work

1. Download the lab4_kit.zip file from the course's web page. The contents of the package is:
   - calculator.v: top-level design file (gray colored in the figure).
   - calculator_tb.v: test bench.
   - arithmetic_unit.v: arithmetic unit that implements the calculator operations.
   - display_ctrl_wrapper.v and display_ctrl.ngc: display controller design.
   - Basys2_100_250_calculator.ucf: generic UCF file.
2. Complete the design of the arithmetic unit to implement the operations described in the above table.
3. Use the provided test bench in calculator_tb.v to verify the design. With icarus verilog you can do:
   - `iverilog *.v`
   - `vpp a.out`
4. Edit the UCF file to make the connections of the signals to the board's devices as depicted in the figure.
5. Bring all the files including your modifications to the lab session!

Lab work

NOTE: have the instructor to check the design after steps 4, 6 and 8.

1. Copy all the lab files to a folder in the lab computer.
2. Create a new project in Xilinx's ISE with name “calculator”. Use Basys2 project properties: General Purpose, Family: Spartan3E, Device: XC3S100E, Package: CP132, Speed grade: -5.
3. Add all the source files to the project, this includes all the “.v” files, the “.ucf” file and the “.ngc” file.
4. Simulate the test bench in ISIM (it is optional if it is already simulated with Icarus Verilog).
5. Execute the synthesis and implementation of the design. Correct the errors, if any, and repeat.
6. Program the design in the FPGA board and test it.
7. Modify the design to make the decimal point between the second and third digits to be on.
8. Modify the design to make one led (LD0) to activate when the result is negative after a subtraction operation (in this case the displayed value is not correct).

Sim.	Test 1	Test 2