The **Microelectronics Training Center**

The MTC is an initiative within the INVOMEC division

Industrialization & Training in Microelectronics

Lab-exercise

Lab 4:

Simulation of the basic HW-SW system

Cluster: Cluster1
Module: Module5d

Target group: Students

Version: 1.1
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http://www.esf-agentschap.be

Introduction

This module presents the first step towards verifying your design. Upon successful design, Micro6 as a microprocessor should be able to run a simple program written in its native assembly language.

Objectives

After completing this module, you should be able to:

- Simulate digital systems

Knowledge background

- Basic knowledge of ModelSim

Classification

- Level: 2
- Duration: 1 hour

Input

- DO Macro
- VHDL files
- Assembly program (`micro_ram_pk.vhd`)

The lab

After building the system architecture in the previous module, you need to check whether the microprocessor operates properly. In the previous module we introduced a short program that sorts an array of integer numbers in a descending order. The array is stored in memory in consecutive locations. The first location indicates the length of the array.

In this module we run this software on our microprocessor. This procedure is not intended to be a full verification of the microprocessor functionality. To that end, sophisticated testbenches have to be designed. The purpose of running a sample program on Micro6 is only to check whether you have successfully integrated the different components of the system. However, there is no systematic way to point out what is wrong in your design. You may need to adopt some intuitive methods for debugging if errors occur.

The sort program is already compiled in the previous module. It resides in the memory contents package `micro_ram_pk.vhd`. To run the program on Micro6, you need first to create a working library. Use the command below for this purpose.

```
vlib work
```

Compile all the VHDL files of the microprocessor. Take into account that some files need to be compiled before others. For example, if a design file uses a package, the package should be

compiled before the design file. You can use the compile.do file to compile all vhdl files of the system in the correct order.

```
Modelsim> do compile.do
```

After you finish compiling all the files, you can simulate your testbench tb_system. In order to verify the correctness of your system you should store the ram contents from address 3000 to 3000+length_of_list before and after executing the “sort” program on the microprocessor.
Since the ram is internally represented by a vhdl variable you cannot look at the ram contents in a waveform or display view. You can use the modelsim command “mem save” in order to write the contents of an array variable in a file.
By setting a breakpoint in control.vhd at the point when the “END” instruction is located you can run the simulation till the “END” instruction is executed.
All the previous commands are stored in the ssort.do file you only have to run it.

```
Modelsim> vsim –do ssort.do
```

`ssort.do` generates two text files showing the list before and after running the program. The two files are `program7_unsorted.txt` and `program7_sorted.txt`, respectively.

Check the results.