by triggering V_{IN} at any constant phase of the 60-Hz power frequency. This procedure always eradicates power-supply ripple effects.

Further illustrating this point: If V_{IN} is a fast pulse triggered at a slight offset frequency, like 61 Hz, a low-jitter pulse will actually meander to-and-fro on the delayed display, at the difference frequency of 1 Hz. Precisely at 60 Hz, the pulse freezes.

To examine a fast transition at higher repetition rates, the transition must be retriggered after the delay. Most commercial delayed-sweep units can do that. The optional passive averaging network in Figure 2 provides just such a delay-qualified trigger function. If ramp T and the V_{IN} transition have equal polarity, then by tuning the LEV knob, E can reliably trigger the delayed scope on that transition—excluding all others. On the other hand, when they're of opposite polarities, one must be inverted before the adding network by an inversion transformer or amplifier.

This network was first tested using a 2-kHz squarewave for V_{IN} to determine the optimum compensation capacitor values of 56 pF. The process is analogous to tuning a low-capacitance probe. To display the resultant E while it externally triggers the delayed oscilloscope, employ a 1-pF, 100-MΩ low-capacitance probe. If plugged into the Tek 515A input, or any other 1-MΩ scope, this 100× attenuation probe will show the V_{IN} signal added to the ramp, while triggering on the desired transition at E. After plugging in V_{IN}, the 515A will display any transition reliably and clearly, with no perceptible jitter.

Cancel Multiplexed DAC's Output Error, And Add A Sign Bit

Antonio Barbancho and Félix Biscarri

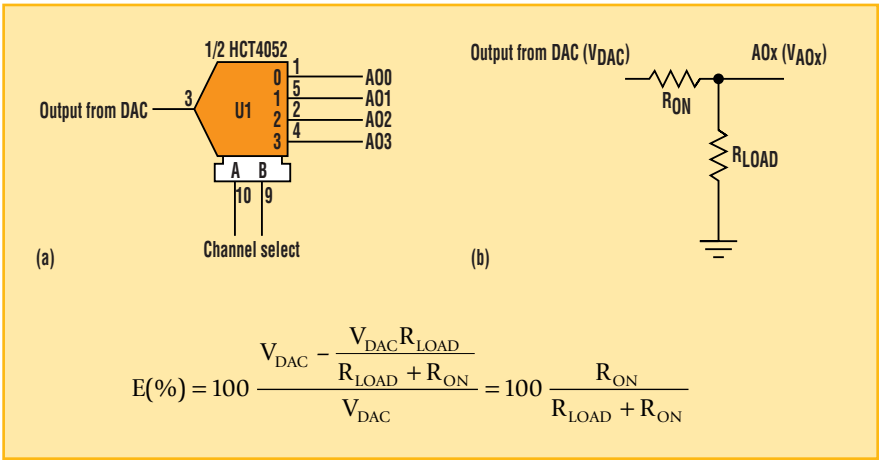
Universidad de Sevilla, Departamento de Tecnología Electrónica, Escuela Universitaria Politécnica, C/ Virgen de África, 7, 41011 Sevilla, Spain

In some applications, like dataloggers, it's desirable to have many multiplexed analog outputs. As only a single output is active at once, a voltage-output digital-to-analog converter (DAC) and an analog multiplexer can do this. You can use this kind of signal to excite bridges. A bipolar output may also be needed, but you don't want to give up a bit of resolution.

To address the first problem, designers usually implement a multiplexer *(Fig. 1a)*. But this arrangement has a serious drawback: The output accuracy could be greatly reduced due to the multiplexer's internal impedance, R_{ON}. Figure 1b shows the added error, E, of AOx, the final output.

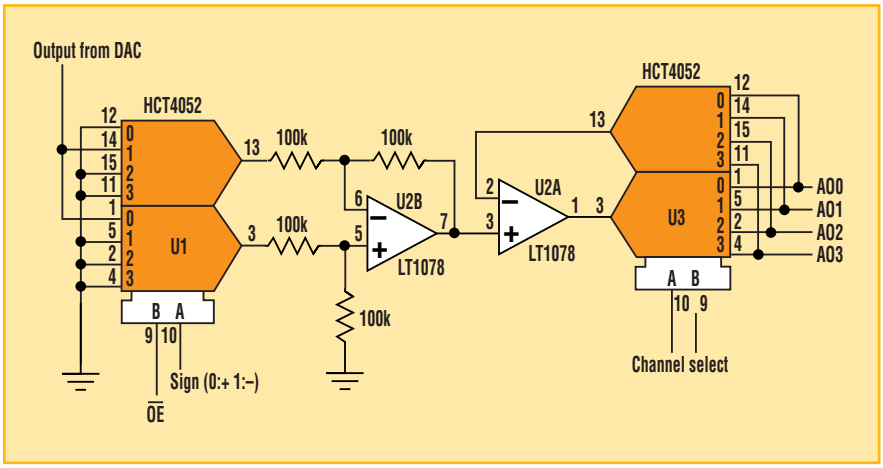
Low-internal-impedance multiplexers (R_{ON} less than 4Ω) are commercially offered at medium prices (about $0.95). Compare this to the HCT4052's R_{ON} (under 280 Ω) that runs $0.10. Alternatively, you can use four op amps to buffer each output.

The circuit of Figure 2 employs an original, low-cost technique to take advantage of the HCT4052's low price. The multiplexer's internal resistance is inserted in the feedback loop of an op amp, and the error, E, is almost cancelled. To add a sign bit, the versatile circuit employs another multiplexer and a unity-gain differential amplifier, which is fed with the DAC's output, or its inverse. This arrangement can be easily modified to add an arbitrary number of outputs by simply changing U3.



$$E(\%) = 100\,\frac{V_{DAC} - \dfrac{V_{DAC}R_{LOAD}}{R_{LOAD}+R_{ON}}}{V_{DAC}} = 100\,\frac{R_{ON}}{R_{LOAD}+R_{ON}}$$

1. A multiplexer is often used with a voltage-output DAC (a). However, the multiplexer's internal resistance (R_{ON}) adds an error to its output voltages, V_{AOx} (b).



2. Inserting the HCT4052's internal resistance in the feedback loop of an op amp almost cancels the output error. Adding a sign bit is accomplished through an additional HCT4052 and a unity-gain differential amplifier.