**Example 2**: calculate f(0,1,1), f(1,0,0), f(1,1,1)

 $f(a,b,c) = (a+b+c) (a + \overline{b} c) + c \overline{(a+c)}$ 

NOT

x z 0 1 1 0

 $z = \bar{x}$ 

AND

ху	Z	
0 0	0	
01	0	
10	0	
11	1 1	

 $z = x \cdot y$ 

$$f(0,1,1) = (0+1+1)(0+11)+1(0+1) \qquad \text{OR} \qquad \frac{\frac{xy}{00}}{\frac{00}{01}} = (1+1)(0+0+1)+1=0 = 1 \cdot (0+0)+1 \cdot 0 = 1 \cdot 0 + 0 = 0 + 0 = 0$$

$$4(1,1,1) = (1+1+1)(1+71)+1(1+1)$$
  
=  $1\cdot 1+0=\frac{1}{2}$ 

## Example 3. Convert to normalized forms of SOP and POS

$$(a+b+c)(ab+\overline{bc})+cd(\overline{a+c})=$$

$$=(a+b+c)ab+(a+b+c)\overline{bc}+$$

$$+cd\overline{a}\overline{c}=aab+abb+abc$$

$$+ac\overline{cd}=ab+abc=ab$$

$$=ab$$

Identity	x+0 = x	x · 1 = x
Commutativity	x+y = y+x	$x \cdot y = y \cdot x$
Distributivity	$x \cdot (y+z) = (x \cdot y) + (x \cdot z)$	$\underline{x+(y\cdot z)} = (x+y)\cdot(x+z)$
Complement	$x+\overline{x}=1$	$x \cdot \overline{x} = 0$

	Idempotence	x+x = x	$x \cdot x = x$
	Complement uniqueness	x is uniq	ue
	Annihilation	x+1 = 1	x⋅0 = 0
	Double complement	$\overline{(\overline{x})} = x$	
	Absorption	x+xy = x	(x+y) = x
	Consensus	$x + \overline{x}y = x + y$	$x \cdot (\overline{x} + y) = x \cdot y$
	Associativity	x+(y+z) = (x+y)+z	$x \cdot (y \cdot z) = (x \cdot y) \cdot z$
$\rightarrow$	De Morgan	$\overline{x \cdot y} = \overline{x} + \overline{y}$	$\overline{x+y} = \overline{x} \cdot \overline{y}$
	Reduction	$xy+x\overline{y}=x$	$(x+y)(x+\overline{y}) = x$

$$(a+b+c)(ab+\overline{b}c)+cd(\overline{a+c}) = (a+b+c)(ab+\overline{b})(ab+c)+cd\overline{c}c = (a+b+c)(a+\overline{b})(a+\overline{b})(a+c)(b+c) = (a+b+c)(a+b)(a+c)(b+c)$$

$$= (a+b+c)(a+b)(a+c)(b+c)$$

$$= (a+b+c)(a+b)(a+c)(b+c)$$

$$= (a+b+c)(a+b)(a+c)(b+c)$$

Example 4. Convert from normalized to canonical forms.

$$a + a\overline{b}c + \overline{b}c =$$

$$\oint_{0}^{1} \int_{0}^{1} \int_{0}^{1}$$

# Example 5. Convert from SOP/POS to truth table

$$z(a,b,c) = a\overline{c} + a\overline{b}c + ac + \overline{b}c$$

$$1$$

$$z = 1 \text{ iif } a\overline{c} = 1 \text{ : } a = 1, c = 0$$

$$abc = 1 \text{ : } a = 1, b = 0, c = 1$$

$$abc = 1 \text{ : } a = 1, b = 0, c = 1$$

$$abc = 1 \text{ : } a = 1, b = 0, c = 1$$

$$abc = 2$$

$$abc = 3$$

$$a$$

$$z(a,b,c) = (a+b+c)(a+\overline{b})(a+c)$$

$$7 = 0 \text{ inf} \quad (a+b+c)=0 \text{ ; } a=0, b=0, c=0$$

$$0 \text{ or } \qquad 0 \text{$$

# Example 6. Algebraic logic expression minimization $xy + \overline{x}y = y$ (Quine-McCluskey simplified method)

$$F(a,b,c,d) = \Sigma(0,1,4,9,11,13,15)$$

 $F(a,b,c,d) = \overline{a} \overline{b} \overline{c} \overline{d} + \overline{a} \overline{b} \overline{c} d + \overline{a} \overline{b} \overline{c}$ 

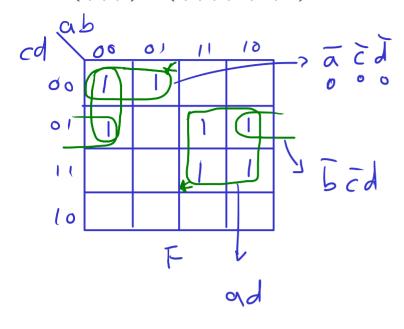
- (we have to use these in our expression)
- («) We need to use one of these also to cover all the minterms.

Two solutions with the same complexity:

1) 
$$F = \bar{a}c\bar{d} + ad + \bar{b}c\bar{d}$$
  
2)  $F = \bar{a}c\bar{d} + ad + \bar{a}\bar{b}\bar{c}$  minimal so P

# Example 7. Logic expression minimization using K-maps.

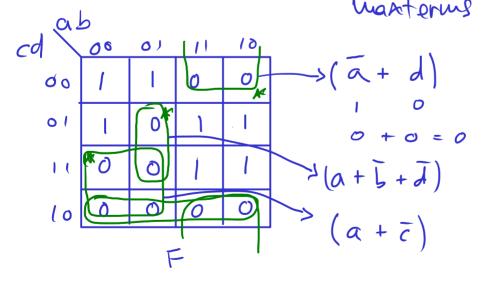
$$F(a,b,c,d) = \Sigma(0,1,4,9,11,13,15)$$



$$F = \overline{a} \cdot \overline{d} + \overline{b} \cdot \overline{d} + ad$$

minimal SOP

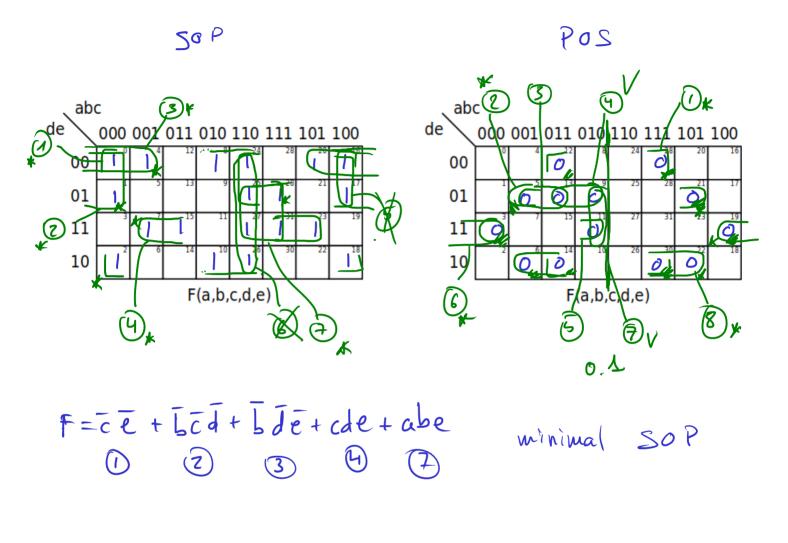
$$F(a,b,c,d) = \Sigma(0,1,4,9,11,13,15)$$



$$\overline{F} = (\overline{a} + d)(\alpha + \overline{b} + \overline{d})(\alpha + \overline{c})$$
 minimal

Extra example: 5 variables K-map minimization.

 $F(a,b,c,d,e) = \Sigma(0,1,2,4,7,8,10,15,16,17,18,20,23,24,25,26,27,28,31)$ 



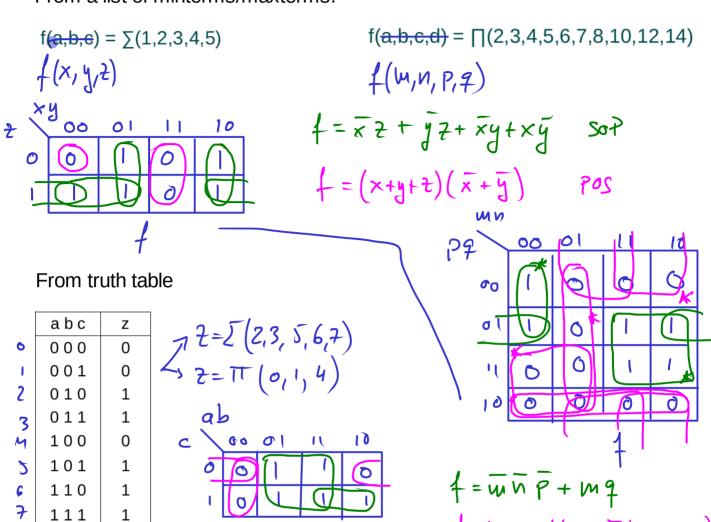
$$F = (\vec{b} + \vec{c} + e)(\vec{b} + \vec{c} + d + \vec{e})(\vec{b} + c + \vec{d} + \vec{e})(\vec{a} + \vec{b} + d + \vec{e}).$$

$$(\vec{a} + \vec{b} + \vec{c} + \vec{e})(\vec{c} + \vec{d} + e) \qquad \text{windual Pos}$$

$$(\vec{a} + \vec{b} + \vec{c} + \vec{e})(\vec{c} + \vec{d} + e) \qquad \text{windual Pos}$$

## Example 8. K-map minimization from different representations

From a list of minterms/maxterms.

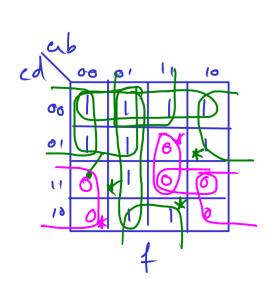


From any expression

$$f(a,b,c,d) = \overline{(a+\overline{b})}(ac+d) + \overline{(b+c)}(\overline{b}+d)$$

4=b+ac

L= (a+b)(b+c)



$$f = \bar{a}b(ac+d) + \bar{b}+c + \bar{b}+d =$$
 $= \bar{a}bd + \bar{b}c + \bar{b}d$ 
 $= \bar{a}bd + \bar{b}c + \bar{b}d$ 
 $= \bar{a}c + \bar{b}c + \bar{b}d$ 
 $= \bar{a}c + \bar{b}c + \bar{b}d$ 
 $= (\bar{a}+\bar{b}+\bar{d})(\bar{b}+\bar{c})$ 

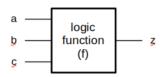
1=(m+p)(m+n)(m+q)

Design an optimum two-levels combinational circuit for example 1 (introduction).

#### Verbal description

A digital alarm system may be on or off and has a presence sensor and a contact sensor at the main door. When the system is on, the alarm will be activated if presence or a door open is detected. When the system is off the alarm is activated only when presence is detected and the door is open (to prevent leaving the door open when at home).

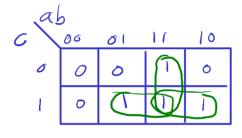
Formal description



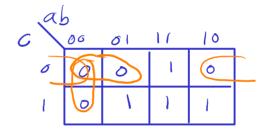
$$z = f(a,b,c)$$

- a (on/off switch): 0-on, 1-off
- b (presence sensor): 0-no presence, 1-presence.
- c (door sensor): 0-door closed, 1-door open
- z (alarm): 0-no activated, 1-activated

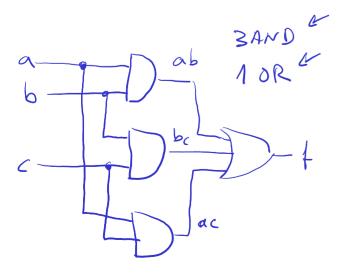
а <u>b</u> ç	Z
000	0
001	0
010	0
011	1
100	0
101	1
110	1
111	1
9	
1	

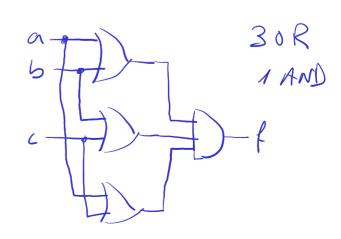


$$cost = 3 + 6 + 0 = 9$$



$$f = (a+b)(b+c)(a+c)$$



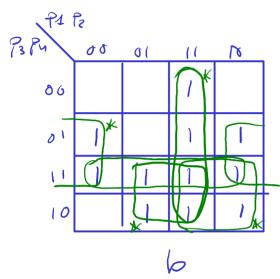


A modern processor run four processing units at a time: P1, P2, P3 and P4. Each unit sets an output bit 'pi' to one when it is busy. The system is considered busy when any of the following conditions is met:

- •P1 and any other unit are busy.
- •P2 and P3 are busy.
- •P4 is busy and neither P1 nor P2 are busy.

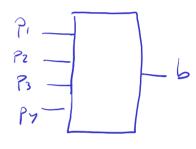
Design a minimum two-level circuit (plus inverters). Inputs are single rail.



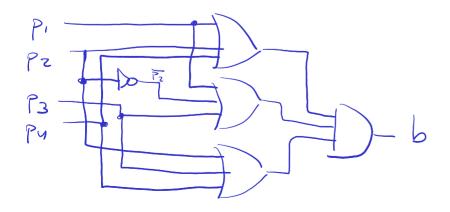


$$b = p_2 P_4 + P_2 P_3 + P_1 P_3 + P_1 P_2$$
  
 $cost = 4 + 8 + 1 = 13$ 

$$b = (p_1 + p_2 + p_4)(p_1 + \overline{p_2} + p_3)(p_2 + p_3 + p_4)$$
  
 $cost = 3 + 9 + 1 = 13$ 



P1:	Pe .				
P3 P4	00	o (	((	16	1
86	0	0	1	VO	_
01	1	O	)	١	
(1)	1	1	1	)	
10	*0	1	1	1	
,	1		  P		,



A modern processor run four processing units at a time: P1, P2, P3 and P4. Each unit sets an output bit 'pi' to one when it is busy. The system is considered busy when any of the following conditions is met:

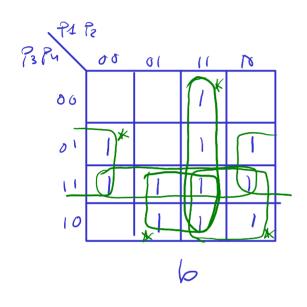
- •P1 and any other unit are busy.
- •P2 and P3 are busy.
- •P4 is busy and neither P1 nor P2 are busy.

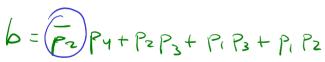
and inverters. Design a minimum two-levels circuit using only NAND gates.

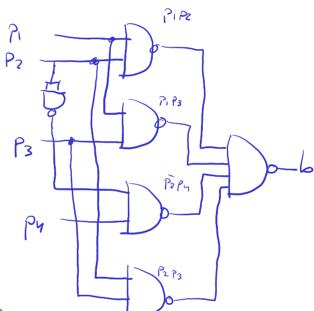


SOP) AMD-OR NAND-MAND

0







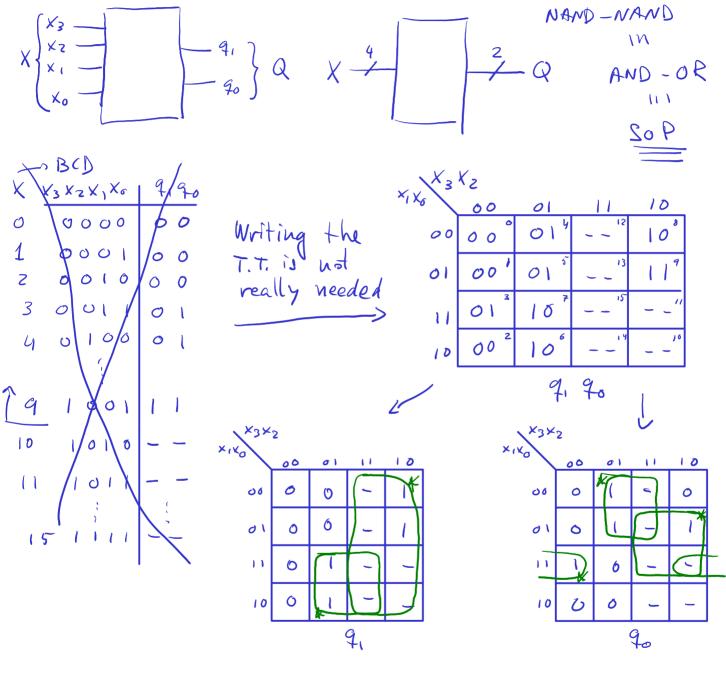
Design a combinational circuit with four inputs (x3, x2, x1, x0) that represent the bits of a BCD-digit X, and two outputs (q1, q0) that represents the bits of a magnitude Q, where q is the quotient of the division X/3.

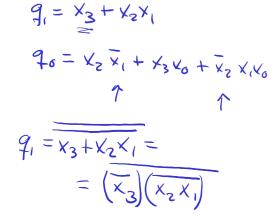
0...9

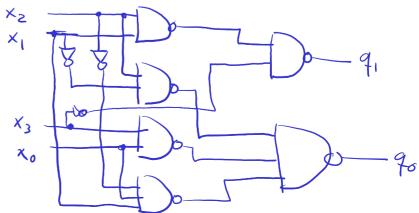
E.g. if X=7  $\rightarrow$  Q=2, that is,  $(x3,x2,x1,x0)=(0,1,1,1) \rightarrow (c1,c0)=(1,0)$ 

0111

Design the circuit using a minimum two-level structure of only NAND gates.





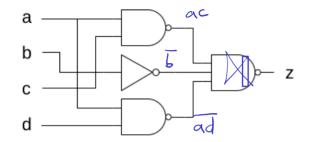


The circuit below corresponds to a damaged alarm system with four inputs and one output. Looking at the connections we know that the inputs correspond to:

- a: system activation (0 off, 1 on)
- b: fire sensor (0 no fire, 1 fire)
- c: front door sensor (0 close, 1 open)
- d: presence sensor (0 no presence, 1 presence)

When output z is active (z=1) the alarm rings.

- Analyze the circuit and obtain its truth table.
- Describe with words the operation of the alarm: cases that make the alarm to ring, etc.
- Redesign the circuit using only NOR gates.



Circuit -> expression -> K-map -> Truth table

Z = ac b ad = ac + b + ad = Verbal description

= ac + b + ad sop NOR - NOR = OR-AND

If alarm is off (a = c)

Soly activates if five (b=1)

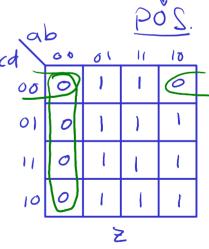
If alarm is on (a=1)

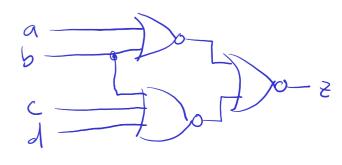
Ring in any sensor

activation

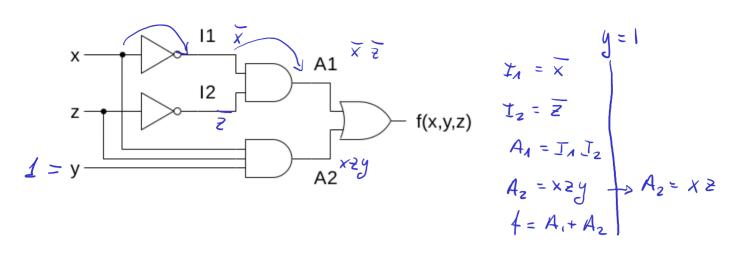
(five, presence, door)

2 = (a+b)(b+c+d)
= (a+b)+(b+c+d)

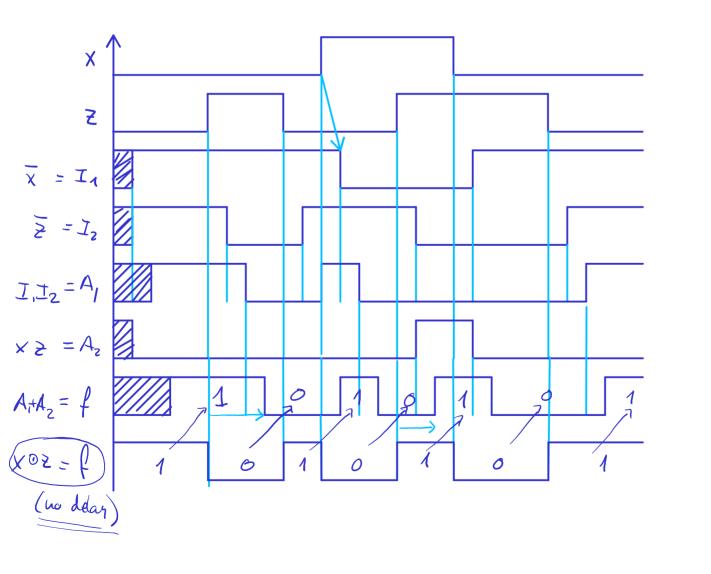




Example 14. Obtain the chronogram of output "f" considering that all gates have the same delay " $\Delta$ ". We know "x" and "z" waveforms and "y=1".

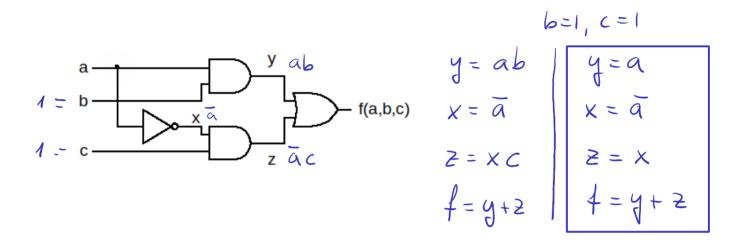


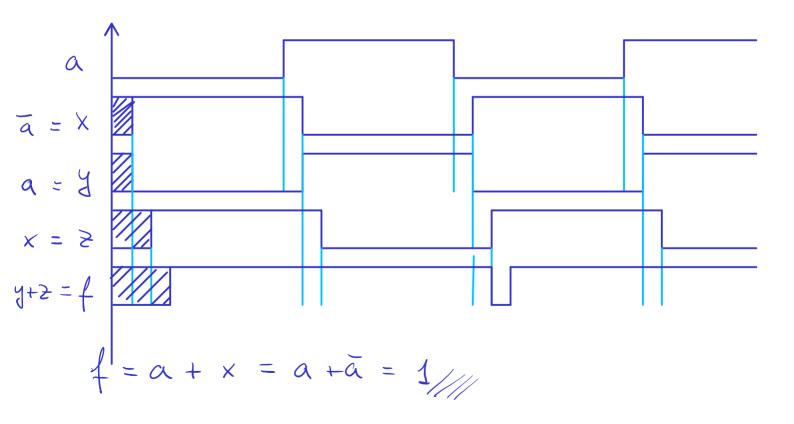
$$4 = x \overline{z} + xyz \qquad f(y=i) = x \overline{z} + xz = x \overline{0} \overline{z} = x \overline{z}$$

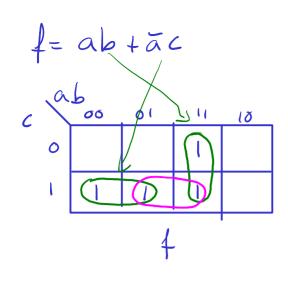


## Example 15. Given the circuit in the picture:

- a) Obtain the chronogram of "f" considering that all gates have the same delay, b=c=1 and that "a" changes periodically.
- b) ¿Does the output present any hazards? If yes, re-desing the circuit to avoid the possibility of output hazards.
- c) Obtain the chronogram of the new circuit to check.



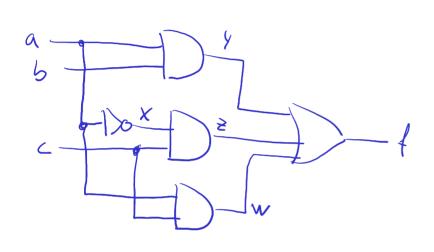




$$f = ab + \tilde{a}c + bc$$

$$|b = c = 1|$$

$$f(b = c = 1) = a + \tilde{a} + 1 = 1$$



$$y = ab = a$$

$$x = \overline{a}$$

$$x = \overline{a}$$

$$x = \overline{a}$$

$$x = \overline{a}$$

$$x = x = x$$

$$x = b = 1$$

$$x = y + 2 + w = 1$$

We can see that f=1 no matter what happens with y or z= there will be no hazards, but we can draw the chronogram to make it more clear  $\sum$ 

X
Y
South with the other circuit,
but not really needed
W
1

1
1