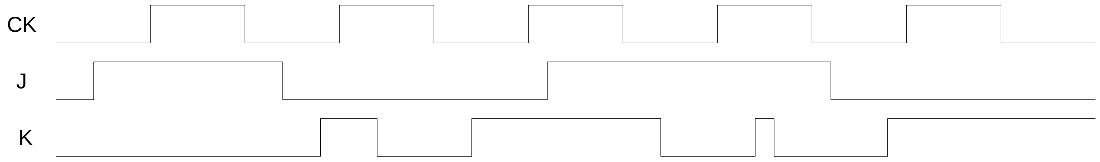
Assignment 6. Sequential circuits

Exercise 1. For the input sequence in the figure, draw the output waveform of:

a) a negative edge-triggered JK flip-flop,

b) a positive edge-triggered JK flip-flop.



Exercise 2. A sequential circuit has an input 'x' and an output 'z' so that 'z' is set to '1' when an input sequence 0-0-1 is detected; and 'z' is set to '0' when the sequence 1-0-0 arrives to the input. In any other case, 'z' preserves its value.

a) Draw the states diagram of a Moore's FSM that solves the problem considering that the overlapping of the sequences is not taken into account.

b) Implement the previous FSM using JK flip-flops and logic gates.

c) Draw the states diagram of a Mealy's FSM that solves the problem considering that the sequences may overlap.

d) Determine if the previous states diagram includes initial states that are only used once. In that case, define an appropriate initial state that allows the removal of these initial states.

e) Implement the Mealy's machine using D flip flops and multiplexers.

f) Write a Verilog description of the Moore's FSM in section a) and a suitable test bench, and simulate the circuit. Use the example at verilog-course.v[1] as template.

Exercise 3. 4-bit groups representing BCD numbers are sent bit-by-bit through a communication line 'x'. The first bit in the group is the least significant bit.

a) Draw the states diagram of a Mealy FSM with an output 'z' that detects when the number 5 is sent through 'x'. Output 'z' must be set (z=1) during just one clock cycle upon detection of the sequence.

b) Design the corresponding sequential circuit that implements the FSM by using JK flip-flops and logic gates.

c) Write a Verilog description of the FSM and a suitable test bench and simulate the circuit. Use the example at verilog-course.v[1] as template.

Exercise 4. We want to design a barrier control system at a car park entrance that uses a single button 'x' to open and close the gate. When the button is pressed, signal 'x' is set to '1' and remains at '0' otherwise. The systems also has an obstacle sensor that controls 'y' so that 'y' is set to '0' when there is an obstacle (a car is crossing under the barrier) and is '1' otherwise. The system generates an output signal 'z' that controls the gate mechanism (0-closed, 1-open).

The detailed operation should be as follows:

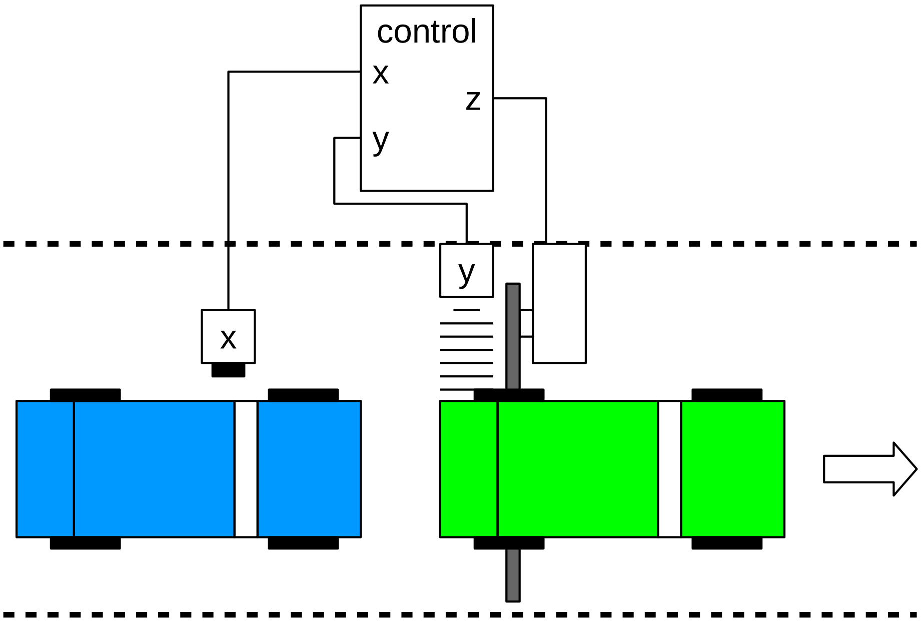
- Starting with the gate closed, the gate should open when signal 'x' is activated.
- The system should wait for the car to cross below the barrier, and close it afterwards.
- If while a car is crossing, a new car arrives and press button 'x', the system should maintain

[1] https://gitlab.com/jjchico/verilog-course.v/tree/master/verilog/06_sequential/06-4_sequences

the barrier open until the new car also crosses the entrance.

a) Design a FSM that solves the problem and implement it using flip-flops and logic gates. Use Mealy's or Moore's style at your own preference.

b) Write a Verilog description of the FSM, a suitable test bench and simulate the circuit.

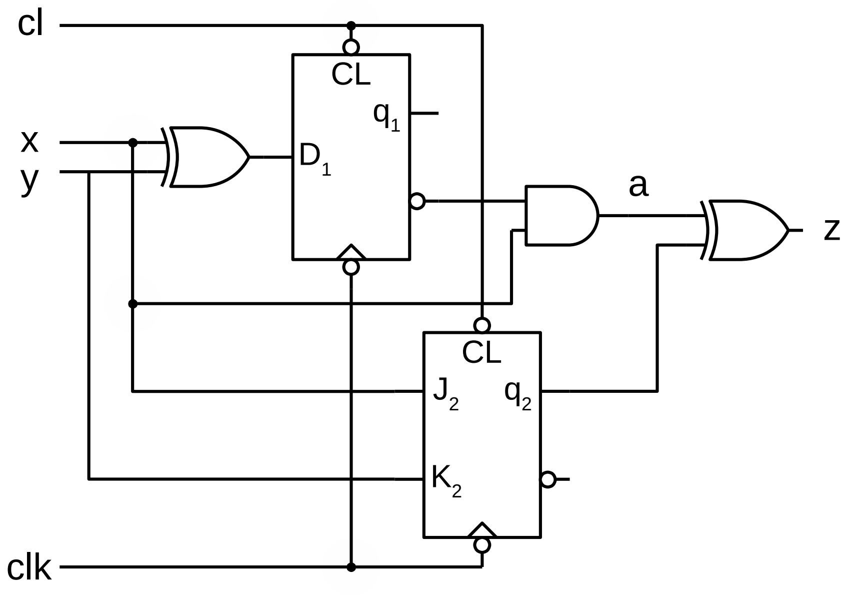


Exercise 5. Analyze the circuit in the figure:

a) Obtains the state diagram of the FSM that it implements.

b) Obtain the waveform of output 'z' for the given input waveforms considering zero delay.

c) Obtain the waveform of output 'z' for the given input waveforms considering the same delay for all devices and output ports.


cl
CL
q_1
x
y
D_1
a
z
CL
J_2
q_2
K_2
clk