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Design of a digital key circuit

Material

- Computer with Xilinx's ISE software installed.
- Digilent's Basys2 prototype board and documentation.
- Sample design files (lab kit).
- Files and documents can be downloaded from the course's web page.

Description

The objective of this lab is to design and implement a basic digital key circuit to control an automatic door. The circuit has an output z so that:

- z = 0: the door is cosed.
- z = 1: the door is opened.

The circuit has four inputs connected to four push buttons: b0, b1, b2 and b3. To open the door (z=1) three of the four buttons have to be pressed (and released) in the following order: b0, b2, b1, that is a numeric key 0-2-1. Once the door is open, it is closed by pressing any button.

The device is a synchronous sequential circuit so it also has a clock input (clk) and a reset input (reset).

In this type of devices that are controlled by push buttons it is very important to consider these two facts:

1. Do not assume that a button is pressed (the input is active) during just one clock cycle: the system clock frequency is 50MHz so the clock cycle is 20ns. If a button is pressed for 1s the system will see that the input active for 50 million clock cycles. So, a repeated input should be considered just as one single code.
2. Push buttons will produce “bounces”. This is the effect that makes the button, when pressed, to close and open several times in a short period of time before finally staying closed. So, a button press is more like “0000010011001110111111111...” than “0000000111111111...”.

The state machine controlling the door should consider these facts. This can be done by following this strategy:

- Move to a new state when the expected button is pressed.
- Stay in that state if all the buttons are released or if the same button is pressed again (it may be a bounce).
- Note that in the unlocking code 0-2-1 consecutive digits are always different. This greatly simplifies the design of the state machine.

Pre-lab work

1. Draw an state diagram of a finite state machine that implements the digital key circuit.
2. Download the lab5_kit.zip file from the course's web page. The contents of the package is:

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- code.v: digital key circuit partial design.
- code_tb.v: test bench.
- Basys2_100_250_code.ucf: generic UCF file.

3. Complete the design of the digital key circuit found in file code.v.
4. Use the provided test bench in code_tb.v to verify the design. With icarus verilog you can do:
   - `iverilog *.v`
   - `vpp a.out`
   - `gtkwave test.vcd`
5. Edit the UCF file to make the connections of the signals to the board's devices as follows:

Circuit port	UCF signal
clk	MCLK
reset	SW7
b[3]	BTN3
b[2]	BTN2
b[1]	BTN1
b[0]	BTN0
z	LD0

6. Bring all the files including your modifications to the lab session!
7. How difficult is it to find the correct key just using the trial and error method?
   a) Calculate the number of combinations that exists with a 3 digits' key without repeating consecutive digits.
   b) Calculate the number of combinations with 4 digits' key.

Lab work

1. Copy all the lab files to a folder in the lab computer.
2. Create a new project in Xilinx's ISE with name “code”. Use Basys2 project properties: General Purpose, Family: Spartan3E, Device: XC3S100E, Package: CP132, Speed grade: -5.
3. Add all the source files to the project, this includes all the “.v” files and the “.ucf” file.
4. Simulate the test bench in ISIM (it is optional if it has already been simulated with Icarus Verilog).
5. Execute the synthesis and implementation of the design. Correct the errors, if any, and repeat.
6. Program the design in the FPGA board and check that the operation is like that in the “Description” section. Check the correct operation of the reset signal in switch 7 (SW7).
7. Modify the design to activate the output with a different 3 digits key. Ask other students to try to find the new key by trying different codes.
8. Modify the design to allow repeated digits. Try with b1, b1, b0. Do not consider bounces.
9. Check for malfunction due to bounces and propose a solution