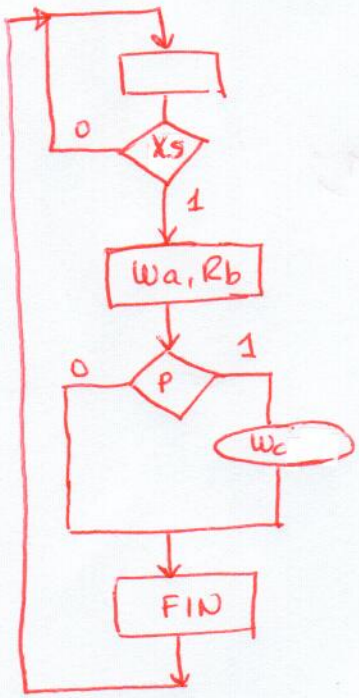
EDC - TI Prueba 2 2016/17

Apartado 1

Carta ASM de la U. control:



Código Verilog

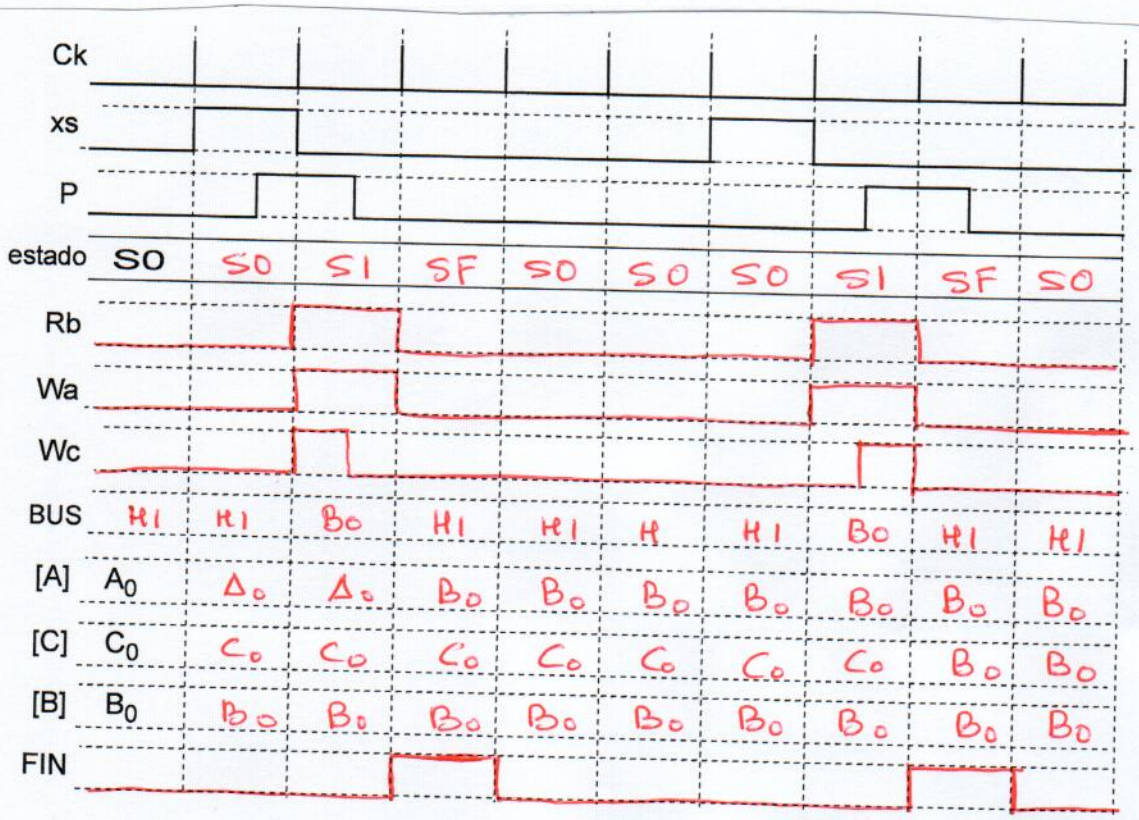
```
module unidad_control(input reset, clk, S, P, output Wa, Wc, Rb, FIN)

parameter S0 = 2'b00, S1 = 2'b01, SF = 2'b10;
reg [1:0] estado_actual, proximo_estado;

always @(posedge clk, posedge reset)
  if (reset == 1)
    estado_actual <= S0;
  else
    estado_actual <= proximo_estado;
```

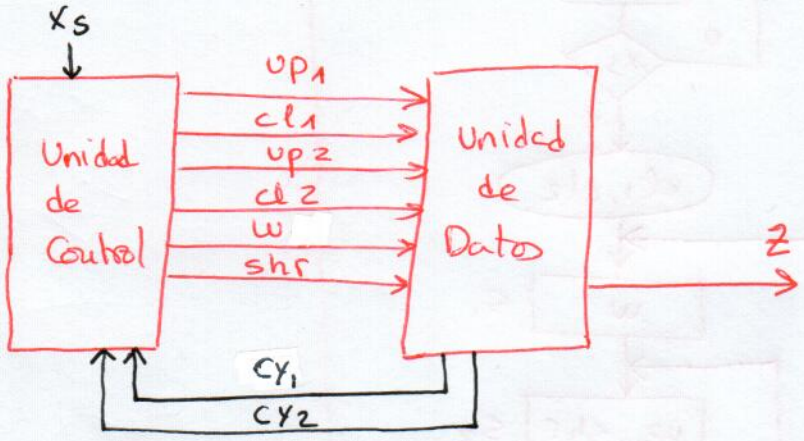
```
always @ (xs, P, estado_actual)
    begin
    {fin, wa, wc, rb} = 0;
    proximo_estado = S0;
    case (estado_actual)
        S0:
          if (xs == 1)
              proximo_estado = S1;
        S1:
          begin
          proximo_estado = SF;
          wa = 1;
          rb = 1;
          if (P)
              wc = 1;
          end
        SF:
          fin = 1;
    endcase
    end
endmodule
```

Diagrama de ondas



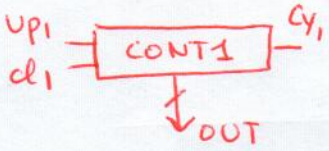
Apartado 2

Esquema del sistema digital



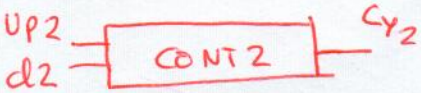
Descripción a nivel RT

CONT 1



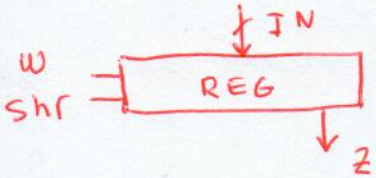
cl_1 up_1	CONT1 ←	OUT =	C_y =
0 0	CONT 1	[CONT1]	1 si
0 1	CONT1 + 1	"	[CONT1] = 255
1 0	0	"	
1 1	proh.	proh	

CONT 2



cl_2 up_2	CONT2 ←	C_y =
0 0	CONT2	1 si
0 1	CONT2 + 1	[CONT2] = 7
1 0	0	
1 1	proh	

REG



w shr	REG ←	z =
0 0	REG	REG[0]
0 1	SHR(REG,-)	"
1 0	IN	"
1 1	proh	"

Carta ASM