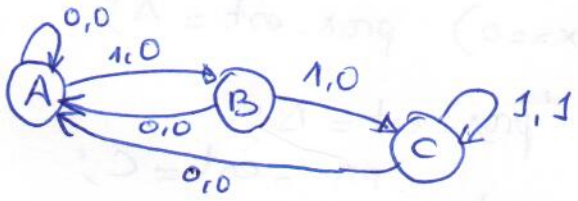
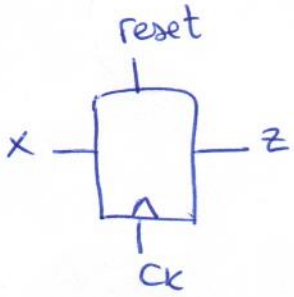
Detector de secuencia de 3 ó más unos mediante Verilog






```
module detector (input x, ck, reset,
                 output z)

parameter A = 2'b00, B = 2'b01,
          C = 2'b10;

reg [1:0] est_presente, prox_est;

always @(posedge ck, posedge reset)
    if (reset)
        est_presente <= A;
    else
        est_presente <= prox_est;

always @(est_presente, x)
    begin
    z=0;
    case (est_presente)
        A: if (x==0)  prox_este= A;
           else  prox_este= B;
```

```
B: if (x==0) prox_est = A;
   else prox_est = C;
default: if (x==0) prox_est = A;
   else begin z=1;
        prox_est = C;
        end
endcase
end
endmodule
```